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- ☐ TN: รายงานเชิงเทคนิค (ฉบับย่อ) (TECHNICAL NOTE)
- ☐ MN: คู่มือการดำเนินงาน (Operation Manual) / คู่มือการใช้งาน (Instruction Manual) / แผนปฏิบัติการ (Operation Plan)

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คำสำคัญ **Keyword**	Pixel Sensor Characterization, Monolithic Active Pixel Sensor, Silicon Sensor

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ดร.กฤษดา กิตติมานะพันธ์	ติดตั้งอุปกรณ์และทดสอบเซนเซอร์ต้นแบบ วิเคราะห์ผลการทดสอบ เขียนรายงานเชิงเทคนิค
นายณัฐวุฒิ เหล่าจำนงค์วงษ์	ติดตั้งอุปกรณ์และทดสอบเซนเซอร์ต้นแบบ
นายเจตนิพิฐ แก้วใจ	ติดตั้งอุปกรณ์และทดสอบเซนเซอร์ต้นแบบ

Abstract

This report presents the laboratory characterization and functional validation of the babyMOSS Monolithic Active Pixel Sensor (MAPS). The testing campaign followed a systematic protocol, starting with fundamental functional verification through power, register, shift register, and DAC scans. Following successful functional verification, the readout system and pixel matrix integrity were validated using digital, analogue, fake-hit rate, and threshold scans. While the sensor was confirmed to be operational, the investigation identified a defect in one of the four regions of the bottom unit, rendering it unreadable. Excluding this damaged area, a comprehensive analysis of the pixel matrices across both the top and bottom regions was conducted to extract key performance metrics. Under specific parameter configurations, the average threshold, noise, and fake-hit rate were successfully obtained. Furthermore, a study was performed to evaluate the sensor performance in operational settings, including IRESET, VCASB, IDB, and Strobe length. The results demonstrate that changes of the sensor performance are consistent with the designed specifications and align with performance benchmarks observed in other babyMOSS sensors. These findings confirm the reliability of the babyMOSS sensor for further experimental integration.

Keywords: Pixel Sensor Characterization, Monolithic Active Pixel Sensor, Silicon Sensor, Stitched Sensor

1. Introduction

The ALICE (A Large Ion Collider Experiment) collaboration at CERN is designed to focus on high-precision measurements of the quark-gluon plasma and to explore the properties of matter at extreme energy densities with higher luminosities during future LHC runs. To achieve this goal, the experiment requires major upgrades of detectors to reach highest performance. One of upgrades is to replace the current Inner Tracking System 2 (ITS2) with the Inner Tracking System 3 (ITS3). It prioritizes an unprecedented reduction in material budget and a closer proximity to the interaction point at 19 mm. As a result, the detector achieves a twofold increase in vertexing and impact parameter resolution when compared to the current ITS, along with higher tracking efficiency for low-momentum particles.

Scheduled for installation during Long Shutdown 3 (LS3) in 2027-2028, the ITS3 upgrade represents a paradigm shift in silicon tracker design. By utilizing 65 nm CMOS technology and fully wafer-scale Monolithic Active Pixel Sensors (MAPS) thinned to approximately 50 μm, the ITS3 will feature sensors bent into a truly cylindrical geometry [1, 2] with ultra-light support and air cooling. This innovation achieves an extremely low material budget of $0.07 X_0$ per layer. This technological foundation also serves as the precursor for ALICE3, a next-generation, fully silicon-based detector architecture designed for the high-rate environments of the 2030s.

One of the ITS3 pixel sensor prototypes is the Monolithic Stitched Sensor (MOSS), designed to validate the performance of the 65 nm MAPS process and the feasibility of large-scale, stitched sensor architectures [3, 4]. The design was submitted to the foundry under the ER1 model. This sensor features a pixel matrix optimized for high spatial resolution (approximately 6 μm) and low power consumption. Previous test beam campaigns have demonstrated that these sensors can achieve detection efficiencies above the designed value of 99%, while maintaining a fake-hit rate below 10^{-6} hit/pixel/event.

Characterizing a babyMOSS sensor, a single unit of MOSS with full functionality, is critical especially when investigation is limited by sensor size, such as radiation hardness testing [5] that establishes the operational envelopes of the sensor in different radiation environments. This involves rigorous laboratory testing to determine how digital and analogue front-end parameters influence sensor stability. By analyzing the threshold, noise, and fake-hit rate, the optimum operating parameters are acquired, directly contributing to the optimization of the final ITS3 and ALICE3 sensor specifications.

2. Objectives

- To verify functionality and the integrity of sensor communication and control circuitry through power, register, and DAC scans.
- To characterize performance and analyze the baseline physical properties of the pixel matrix, specifically the average threshold, noise distribution, and fake-hit rate.
- To assess the uniformity of the sensor response across the top and bottom units and identify any non-functional or damaged regions.
- To investigate parametric sensitivity and the influence of internal DAC parameters—specifically IRESET, VCASB, IDB, and Strobe length—on the fake-hit rate.
- To compare the experimental findings with the chip designer's expectations and existing performance data from related MAPS prototypes to ensure consistency in the 65 nm fabrication process.

3. The MOSS Architecture

3.1 MOnolithic Stitched Sensor (MOSS)

The MOnolithic Stitched Sensor or MOSS is a full-size wafer-scale prototype developed for the ALICE ITS3 upgrade. To achieve the goal of a "wafer-scale" sensor that can be thinned and bent into a truly cylindrical geometry, the MOSS employs a technique known as stitching. Since standard CMOS manufacturing is limited by the "reticle size" (the maximum area a lithography machine can print in one step), stitching allows multiple reticle designs to be connected seamlessly across the silicon wafer, creating a single, continuous monolithic sensor much larger than the standard limit.

- Physical Dimensions: The MOSS measures approximately 14 mm x 259 mm.
- Total resolution: 6.7 megapixels.
- Modular Design: It consists of 10 Repeated Sensor Units (RSUs). Each RSU functions as a modular block of the pixel matrix, sharing common power and control lines across the stitched interface. It can also be powered via pads from the long edge individually or via a metal stripe across all units to the left and right end-caps.

Figure 1 illustrates the MOSS sensor mounted on the carrier board with five connectors and Figure 2 shows the structure of the MOSS sensor divided into ten RSUs together with readout channels via long edges and end-caps.

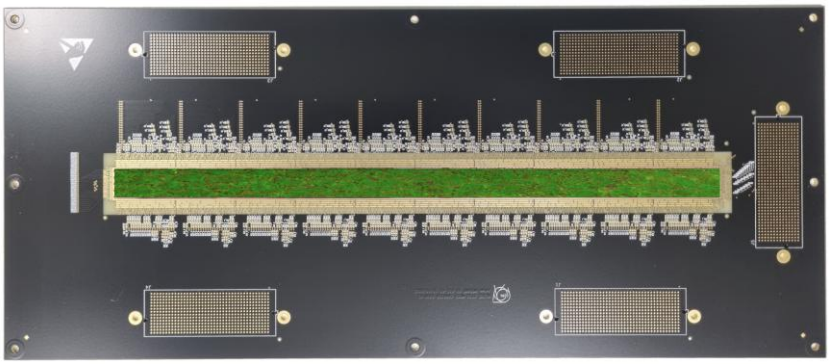

Figure 1 Monolithic Stitch Sensor or MOSS (green area) attached on a carrier board with five interface connectors.

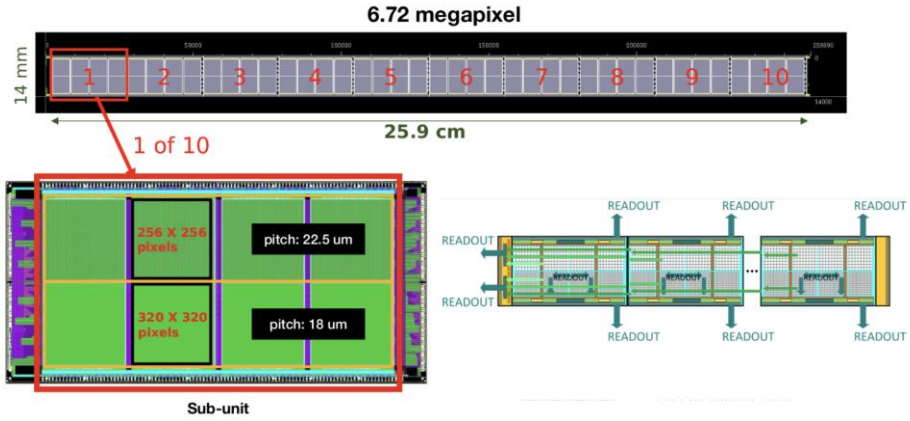

Figure 2 Structure of the MOSS sensor divided into ten Repeated Sensor Units (RSUs) and structure of each RSU and its readout channels.

3.2 The babyMOSS Prototype

The babyMOSS is a specific R&D vehicle designed to test the performance of a single RSU in parallel with the validation of the full-sized MOSS. It serves as a vital tool for characterizing the pixel matrix and front-end electronics required for ITS3. Figure 3 displays a schematic map to produce MOSS and babyMOSS sensors on a single wafer of 300 mm in diameter [6]. Six MOSS sensors are produced in the middle of the wafer, while 23 babyMOSS sensors are produced where the full length

is shorter than the wafer diameter. Each babyMOSS, acting as a single RSU, is divided into two distinct functional regions:

1. Top unit with a pixel matrix consisting of 256 x 256 pixels and a pitch size of 22.5 μm.
2. Bottom unit with a pixel matrix consisting of 320 x 320 pixels and a pitch size of 18 μm.

By isolating a single RSU, researchers can perform high-granularity studies on the analogue and digital front-ends. This includes measuring the threshold dispersion and noise occupancy without the complexity of the full-scale 10-RSU data transmission.

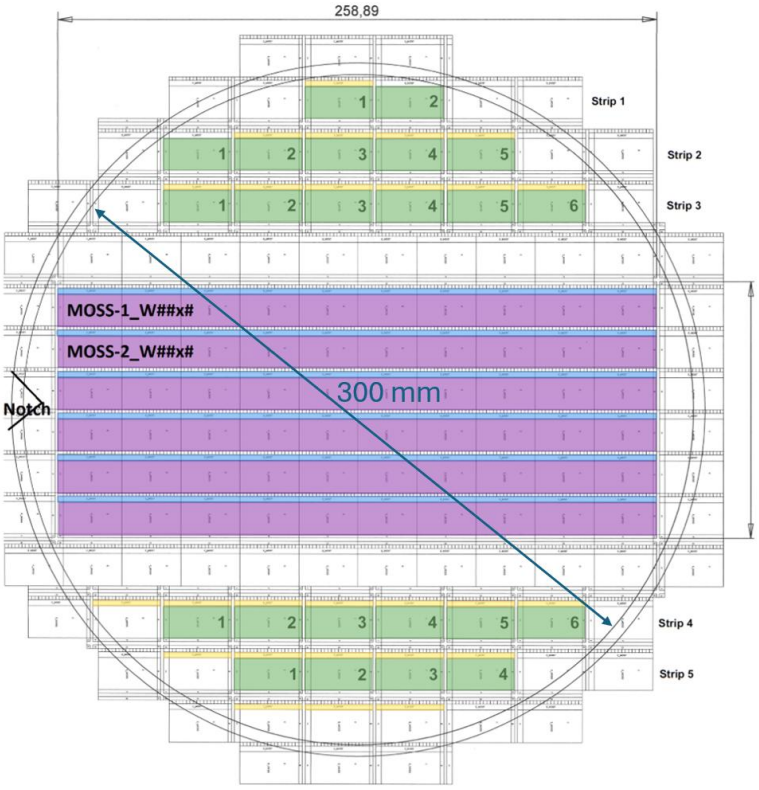

Figure 3 Schematic map for production of the six MOSS sensors in the middle and 23 babyMOSS sensors on a 300-mm wafer.

3.3 Pixel Circuitry and Front-End

The sensor front-end is designed to bias a collection diode and amplify signals with a threshold to determine pixel hits. Figure 4 depicts the analogue in-pixel front-end diagram of the MOSS sensor. A collection diode (D0) receives signals from electrons directly generated from the hits, while M1 and M2 transistors amplify output signals [6]. The operating mode is mainly controlled by four currents IBIAS, IBIASN, IRESET, and IDB, and four voltages VCASB, VCASN, VSHIFT, and VRCAS. Key parameters to investigate in the laboratory are:

- I_{RESET}: A current in a pico-ampere range to reset the collection diode.
- V_{CASB}: A voltage that controls the baseline voltage at the amplifier output and allows the threshold tuning of the pixel matrix.
- I_{DB}: A discriminator current of the amplifier output signal to adjust the threshold of the charge-collection diode.
- STROBE: A parameter to define the time window during which the sensor is sensitive to "hits," directly impacting the fake-hit rate.

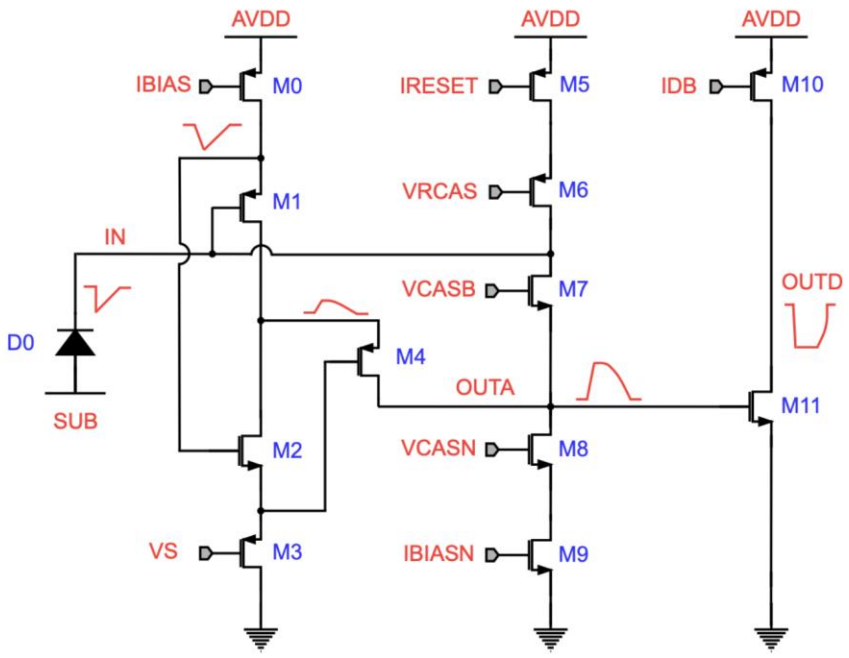

Figure 4 Simplified diagram of the analogue in-pixel front-end of the MOSS sensor.

4. Methodology

The test setup to investigate the babyMOSS prototype, illustrated in Figure 5, primarily consists of a Data Acquisition (DAQ) board, a Raiser card, and a babyMOSS sensor of 14 × 25.9 mm, attached and wire-bonded onto the Carrier board. The DAQ board, the Raiser card, and the babyMOSS sensor IDs are given in Table 1. Due to the fragility of wire-bonding, a custom plastic frame is utilized to protect this delicate connection from accidents, leading to damage or short circuits. Furthermore, this housing serves as a shield, ensuring that ambient light does not interfere with the pixel matrices during testing. When using the Raiser card for the first time, the voltage between AVDD and DVDD must be adjusted by two potentiometers to 1.2 V and two pins must be connected to the carrier board NTC sensors (see Figure 5). A zero-ohm shunt is connected to the "SUB" channel on the DAQ board when operating without reverse bias voltage and a filter board is required if PSUB is applied. The DAQ board is externally powered by +5V and 500-mA current. To communicate between the hardware test setup and the PC, FX3 and FPGA firmware must be installed (see Appendix A for firmware installation and testing scripts) [6, 7].

Signal communication between the Carrier board and the primary DAQ system is facilitated by the Raiser card. This Raiser card was specifically engineered as a compact interface for the single-RSU babyMOSS, serving as a specialized alternative to the larger Proximity Card used for full-scale MOSS sensors. The DAQ board acts as the central hub of the system, connecting to a host computer via a USB connection to execute control commands and log readout data. This operation is managed through a proprietary software suite developed by the research team.

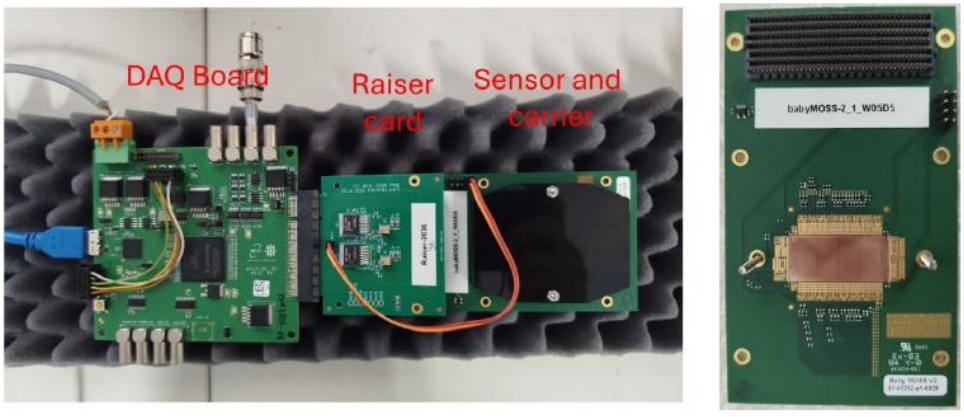

Figure 5 Setup to investigate the functionality of the babyMOSS sensor (left), consisting of a DAQ board, a Raiser card, and a babyMOSS sensor on a carrier card (right).

Table 1 DAQ, Raiser card, and babyMOSS IDs used in this test.

Item	ID
DAQ board	TUM-2024-04
Raiser card V2	2036
babyMOSS sensor	babyMOSS-2_1_W05D5

Table 2 Initial parameters used to study functionality of the babyMOSS sensor in the laboratory.

Parameters	Value
IBIAS	62
IBIASN	100
IDB	50
IRESET	10
VCASB	15
VCASN	64
VPULSEH	64
VSHIFT	192

Once the setup is ready, functional testing, readout and pixel matrix testing, and parametric scan can be performed. The functional test is carried out to verify the fundamental communication and control infrastructure of the sensor; it includes power-on scan, register scan, shift register scan, and DAC scan. After successful testing of sensor functionality using default values in Table 2, the readout and pixel matrix can be tested to evaluate the integrity of the data path and the physical pixel matrix. The tests include digital, analogue, fake-hit rate, and threshold scans. The successful results of these scans ensure that the babyMOSS and its setup can operate properly and are ready for further characterization. After that, the parametric scan of IDB, IRESET, and Strobe length can be conducted to determine sensor performance under different operational configurations.

5. Results and Discussion

5.1 Functional testing includes power-on scan, register scan, shift register scan, and DAC scan.

5.1.1 The **power-on scan** is performed with and without the carrier board to monitor the current consumption as the sensor is energized to ensure there are no short circuits and that the

power-up sequence is stable. The power-on scan was successful and output power status with proper AVDD, DVDD, and IOVDD currents.

5.1.2 The **register scan** verifies the integrity of the configuration registers by performing "write-read-compare" operations to ensure the sensor can store operational settings. The scan result was successful.

5.1.3 The **shift register scan** tests the serial communication path used to load configuration data into the pixel matrix, ensuring that bits are shifted through the long chains without corruption. The scan result was also successful.

5.1.4 The **DAC scan** measures the output of the internal Digital-to-Analogue Converters (DACs) to confirm they provide the correct biasing voltages and currents for the pixel front-end. The DAC scan was successful.

5.2 Readout and pixel matrix testing includes digital, analogue, fake-hit rate, and threshold scans.

5.2.1 The **digital scan** injects a digital signal directly into the end of the pixel front-end to verify that the digital readout circuitry, including hit-encoding and data transmission, is fully functional. The result was successful.

5.2.2 The **analogue scan** injects a charge into the analogue input node of each pixel to test the entire chain (preamplifier, discriminator, and readout). This helps identify "dead" or unresponsive pixels. The result was successful.

5.2.3 The **fake-hit rate scan** measures the number of hits recorded in the absence of an external source or particle beam. This determines the intrinsic noise occupancy of the sensor. Figure 6 depicts the fake-hit rate map of the top and bottom regions of the babyMOSS sensor. By scanning individual region at a time, it is found that region-2 of the bottom unit is damaged due to excessively high fake hits.

5.2.4 **Threshold Scan** injects pulses of varying charges to determine the "S-curve" for each pixel, allowing for the extraction of the mean threshold and the equivalent noise charge. Figure 7 illustrates the threshold distribution of the top and bottom regions of the babyMOSS sensor. The study reveals that the average thresholds of the top unit range between 25.50 – 30.01 DAC. In contrast, the average thresholds measured for the bottom unit range between 20.49 – 21.92 DAC. It should be noted that the second region of the bottom unit (B2) was unable to yield threshold values due to an excessively high fake-hit rate. Threshold scan also provides noise distribution, displayed

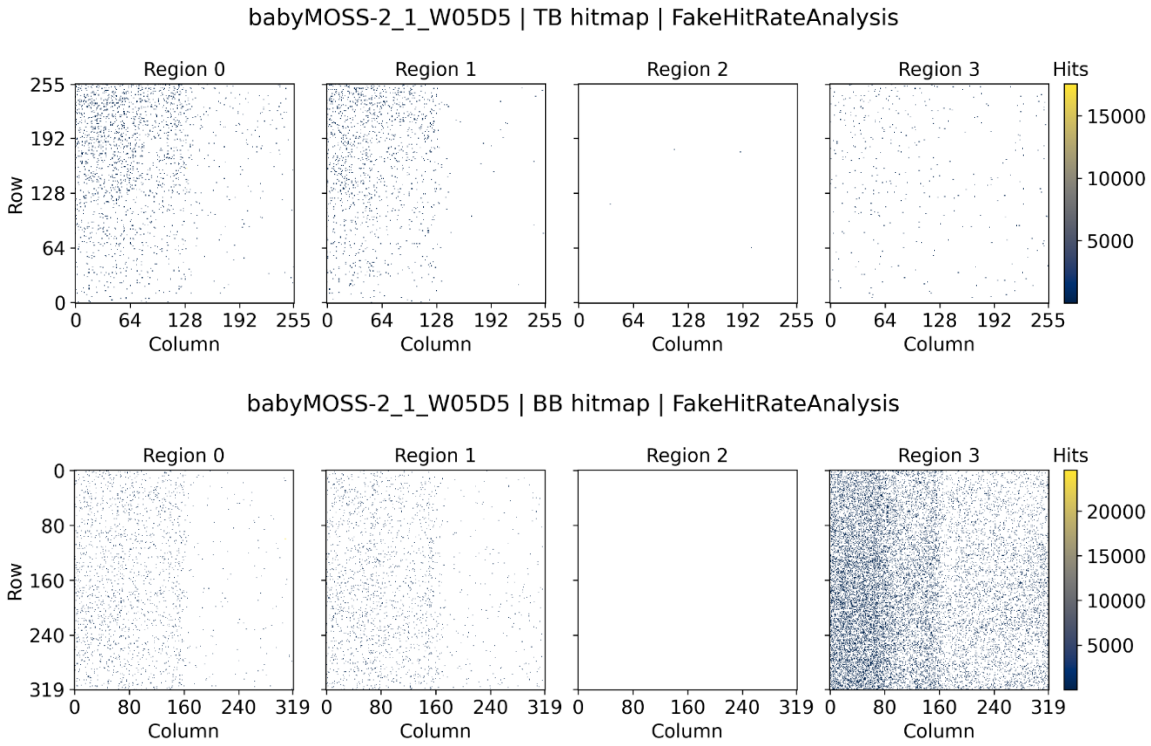

Figure 6 Fake hit map of the top and bottom regions of the babyMOSS sensor.

in Figure 8. The top unit exhibits consistent average noise levels ranging between 2.83 – 2.90 DAC. Similarly, the functional regions of the bottom unit show consistent average noise levels between 2.57 – 2.87 DAC. Similar to the threshold measurements, the region B2 was also unable to provide data regarding noise distribution.

5.3 Parametric scan: IDB scan, IRESET scan, and Strobe length scan

5.3.1 **IRESET Scan** evaluates the impact of the reset current (IRESET) on the analogue pulse shape and the time it takes for a pixel to return to its baseline. Figures 9 and 10 display the relations of fake hit rates as a function of IRESET for different VCASB values of the top and bottom regions. The relationship between the fake-hit rate, the VCASB voltage (used to tune the sensor's data acquisition threshold), and the IRESET bias current were investigated for both the top and bottom units. As illustrated in the scan results comparing VCASB values from 14 to 26 DAC against IRESET values from 6 to 15 DAC, a consistent trend emerged across the entire sensor: the fake-hit rate decreases as the IRESET current increases. In both units, the highest fake-hit rate levels were recorded at the minimum IRESET of 6 DAC and the maximum VCASB of 26 DAC, while the most stable performance with the lowest fake-hit counts occurred at a VCASB of 14 DAC.

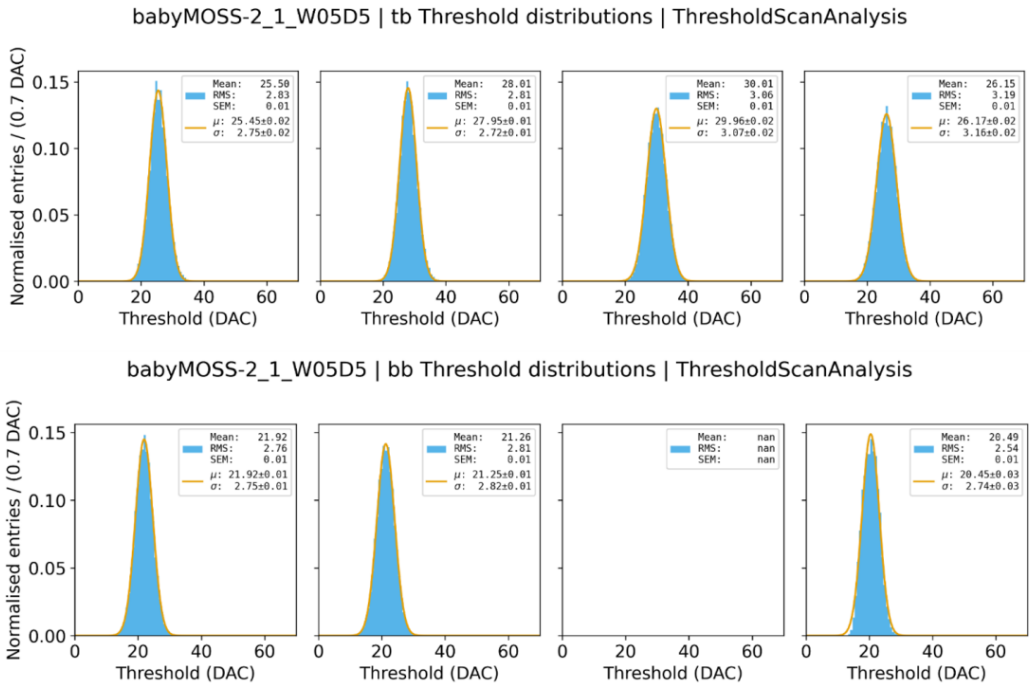

Figure 7 Threshold distribution of the top and bottom regions of the babyMOSS sensor.

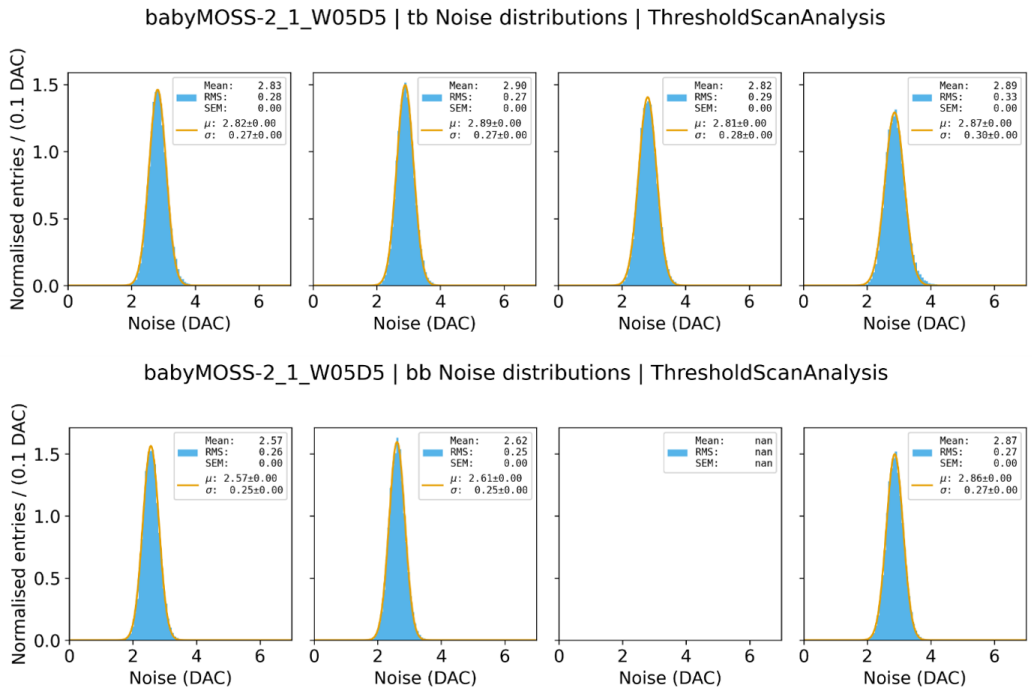

Figure 8 Noise distribution of the top and bottom regions of the babyMOSS sensor.

Detailed analysis of the individual sub-units within the top unit revealed that specific transistor architecture significantly influenced these fake-hit rate characteristics. For instance, T0, which utilizes standard transistor sizing, showed a relatively small fake-hit rate response to changes in VCASB, yet it maintained the highest overall fake-hit rate throughout the study. In contrast, T1 (featuring larger Input Transistors) demonstrated a sharp reduction in fake-hit rate as IRESET transitioned from 8 to 10 DAC, a behavior that became increasingly pronounced as VCASB was lowered to 14 DAC. T2, incorporating larger Discriminator Input transistors, exhibited the lowest overall fake-hit rate, achieving zero fake hits at configurations such as VCASB 14 DAC with IRESET > 10 DAC. Proven to possess the lowest fake-hit rate, the T2 structure will be further considered as the baseline for the following sensor design. Finally, T3 (utilizing larger Common-Source transistors) displayed the most significant fake-hit rate fluctuations compared to other units for identical IRESET settings.

The bottom unit exhibited similar overall trends, though with distinct sub-unit variations. The B1 sensor demonstrated a lower fake-hit rate than B0 once the VCASB voltage exceeded 20 DAC, while the B3 sensor consistently showed the highest fake-hit rate across the range. Notably, the bottom unit results did not display the abrupt, sharp decline in fake hits that was observed in the T1 sensor at VCASB settings of 18 DAC or lower. These variations confirm that the deliberate modifications to transistor sizing—whether standard, increased input, discriminator input, or common-source—directly dictate the noise occupancy and operational stability of the MAPS matrix across different regions of the babyMOSS sensor.

5.3.2 **IDB Scan** investigates how varying the discriminator bias current (IDB) affects the switching speed and global threshold, directly influencing the fake-hit rate. Figures 11 and 12 illustrate relations of fake-hit rates as a function of IDB for different VCASB values of the top and bottom regions. In addition to the previous studies, the relationship between the fake-hit rate, VCASB, and the IDB current—which controls the discriminator stage of the front-end circuit—was investigated.

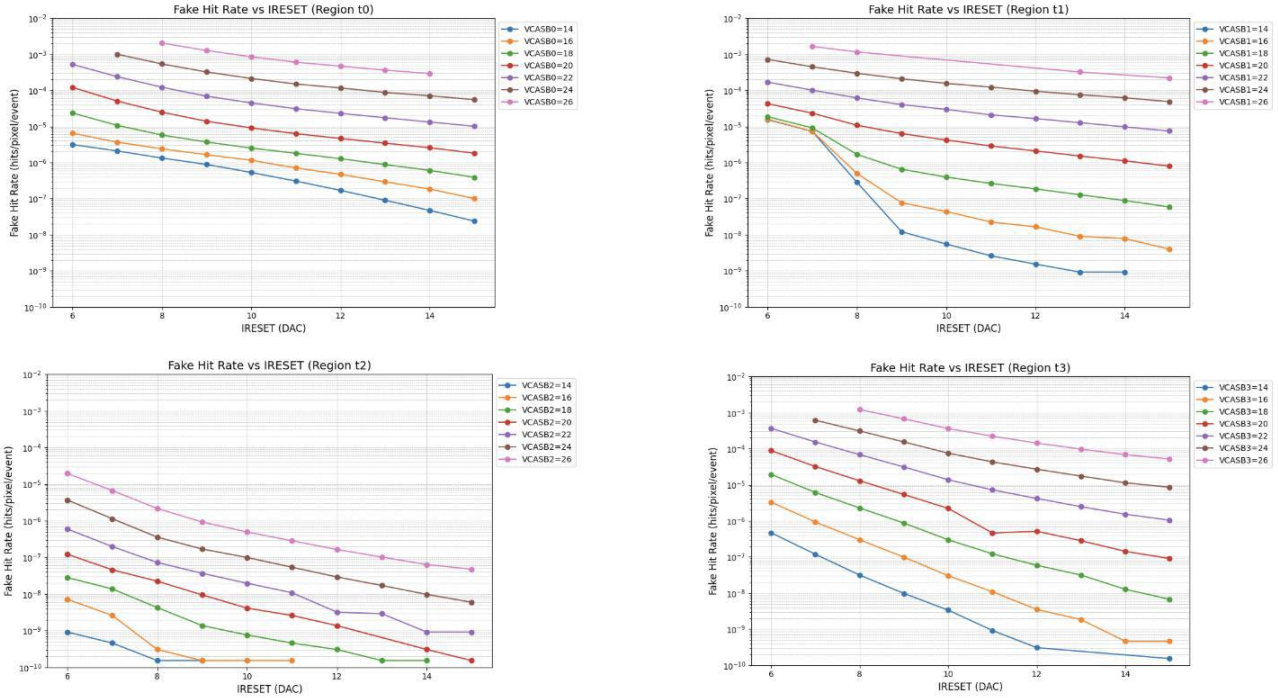

Figure 9 Relations of fake-hit rates as a function of I_{RESET} for different VCASB values of the top regions.

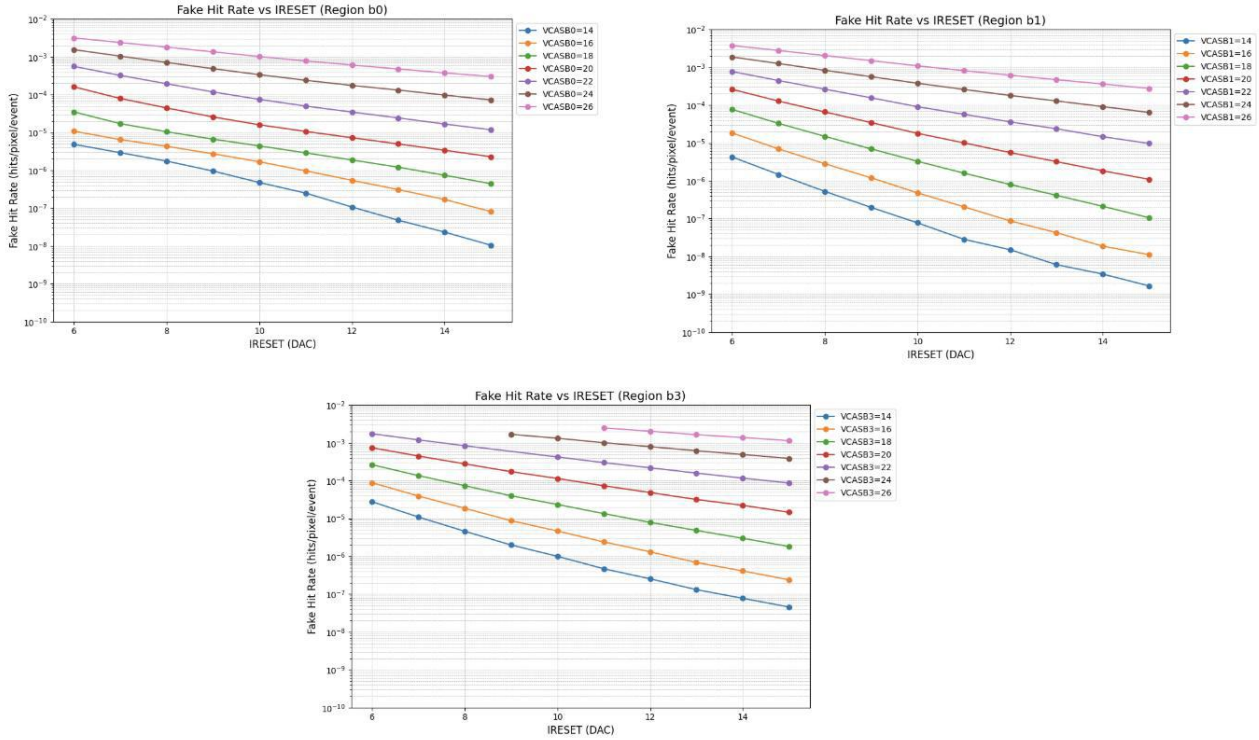

Figure 10 Relations of fake-hit rates as a function of I_{RESET} for different VCASB values of the bottom regions.

Across the top unit sub-units, it is evident that the fake-hit rate decreases as the IDB current increases. The maximum fake-hit rate was observed at an IDB of 40.0 DAC, while the minimum was recorded at 60.0 DAC. When analyzing the impact of the threshold tuning voltage, the fake-hit rate increased proportionally with VCASB. Among the sub-units, T0 exhibited the highest fake-hit counts, whereas T3 demonstrated the lowest. Notably, unlike the IRESET scans shown in Figure 9, the IDB current adjustments did not produce the abrupt, sharp decline in fake-hit rate previously observed in the T1 sensor.

The bottom unit displayed a characterization profile nearly identical to that of the top unit regarding the interplay between fake-hit rate, VCASB, and IDB. The fake-hit rate consistently decreased with higher IDB current. Within this unit, the B1 sensor achieved its minimum fake-hit rate when VCASB was set to 14 DAC. These results further confirm that while IDB is a powerful tool for global threshold management, its effect on specific transistor architectures like T1 is more linear compared to the reset current.

5.3.3 **Strobe Length Scan** adjusts the duration of the integration window to find the optimal balance between catching real particle hits and minimizing the accumulation of fake hits. Figure 13 depicts the relations of fake-hit rates as a function of Strobe length for different VCASB values of the top and bottom regions as the Strobe length varied from 1 to 10,000 and VCASB ranged from 10 to 25 DAC.

In the top unit, the fake-hit rate generally increases with the Strobe length until it reaches a saturation point. This plateau is most evident in sub-units T0, T1, and T3. Specifically, T0 exhibits this behavior consistently across all VCASB settings, whereas it only becomes prominent in T1 and T3 at higher VCASB values of 20 and 25 DAC. Notably, T0 and T1 showed a significant surge in fake hits when the Strobe length was within the 40–80 Clock Cycle (CC) range. In the shorter Strobe length region (10–30 CC), the response of T2 and T3 deviated from expected trends, and the sensor encountered difficulties in logging reliable fake-hit rate data between 10–40 CC. These variations are directly attributed to the distinct transistor designs implemented in each sub-unit.

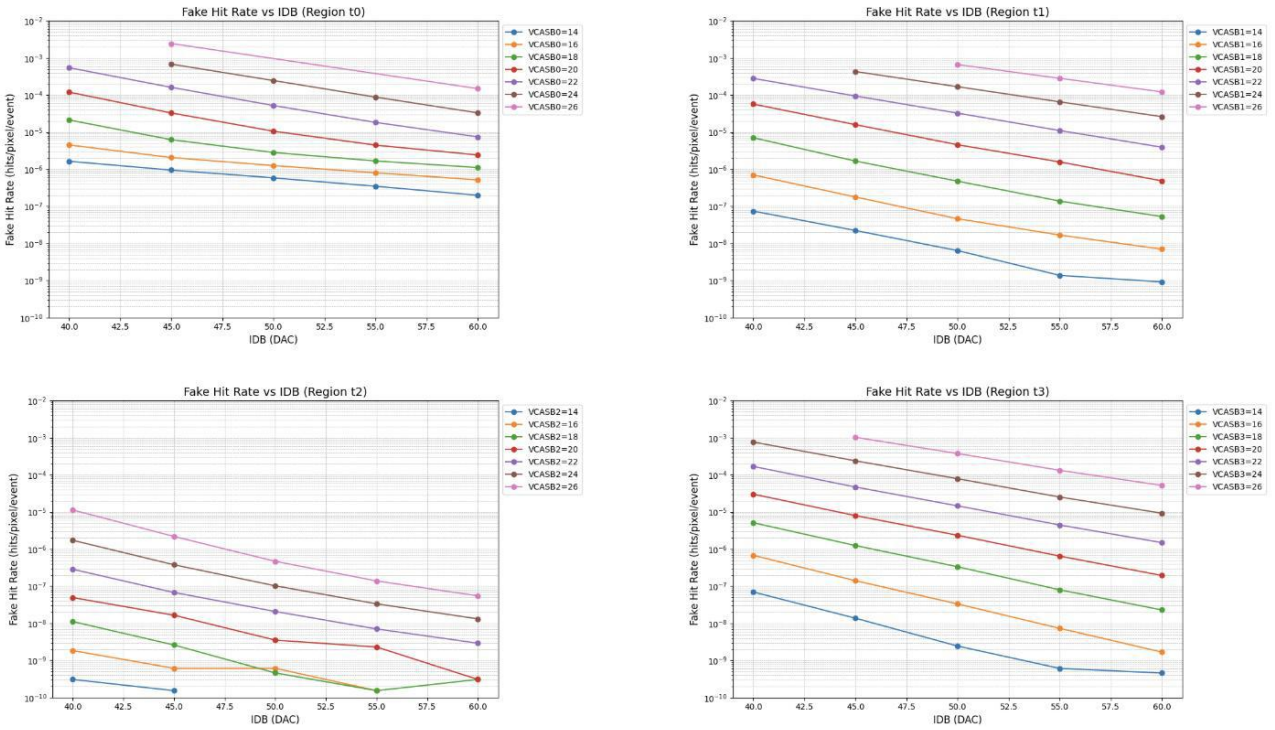

Figure 11 Relations of fake-hit rates as a function of I_{DB} for different VCASB values of the top regions.

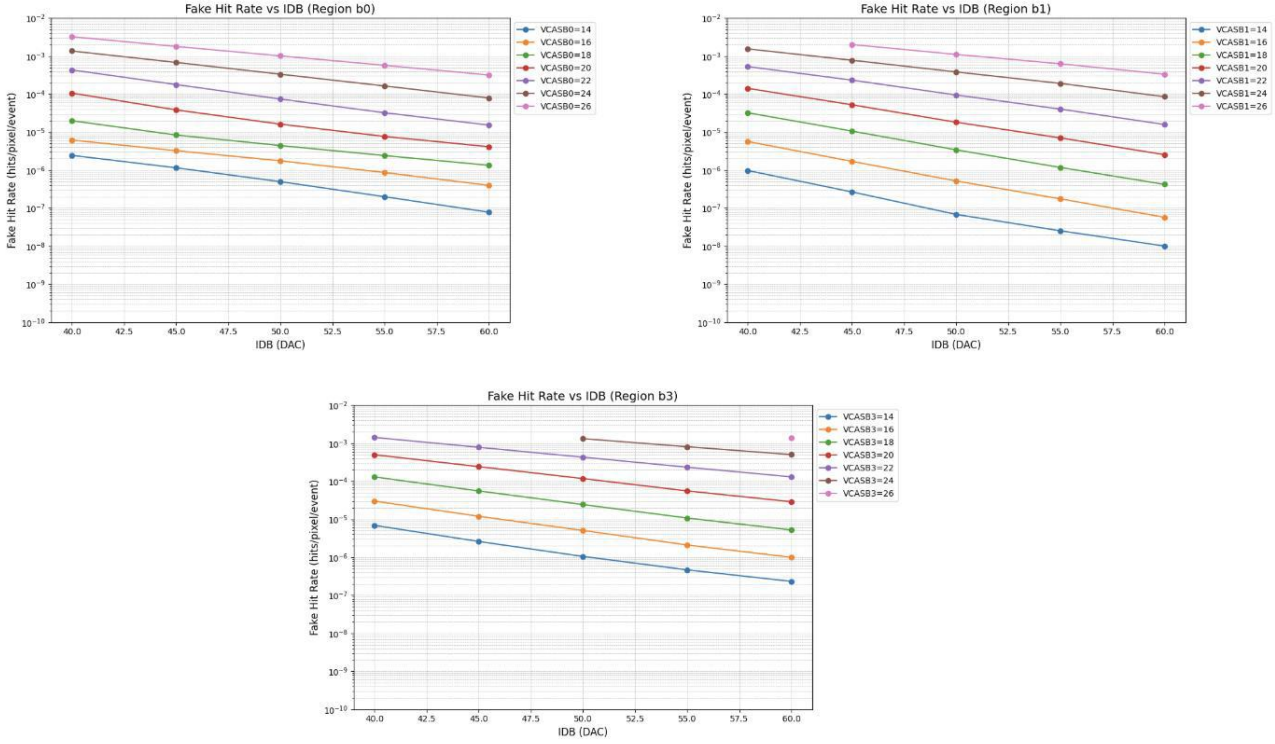

Figure 12 Relations of fake-hit rates as a function of I_{DB} for different VCASB values of the bottom regions.

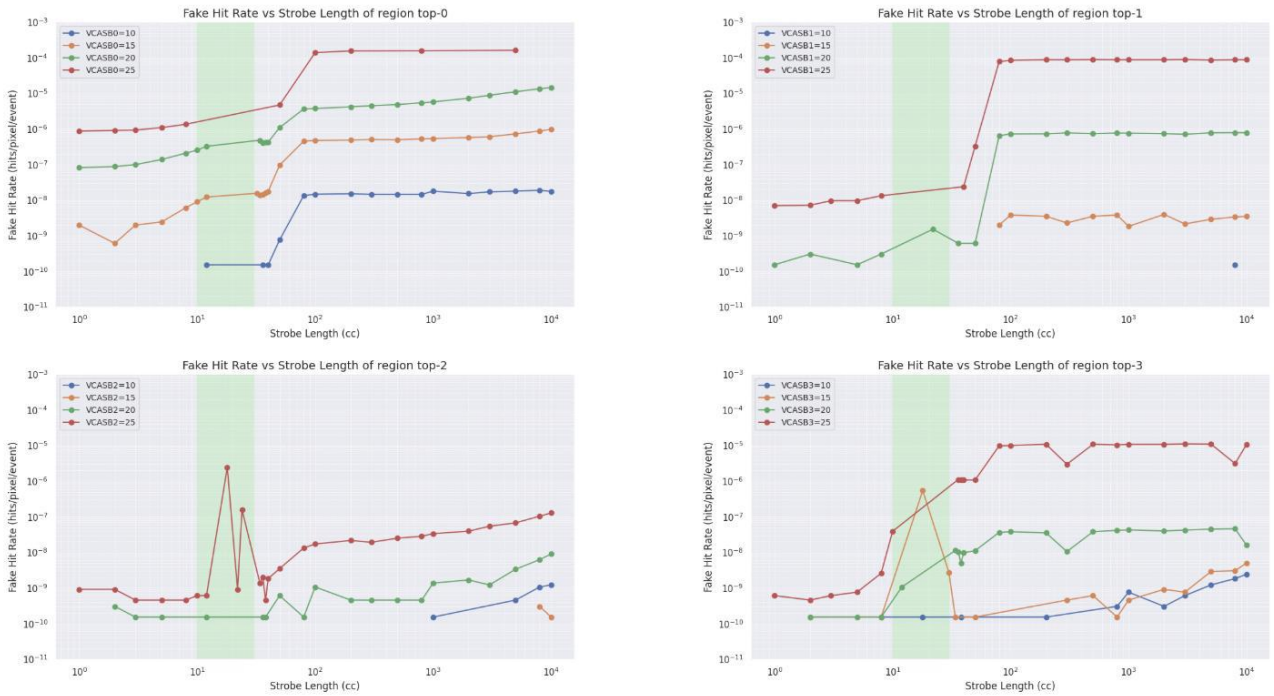

Figure 13 Relations of fake-hit rates as a function of Strobe length for different VCASB values of the top regions.

The bottom unit characterization provided more predictable results that contrasted sharply with those of the top unit, particularly in the short-duration window. For all bottom sub-units, a rapid and clear increase in fake-hit rate was observed when the Strobe length was between 10–30 CC. While B0 exhibited a single significant increase in fake hits, both B1 and B3 demonstrated a dual-step increase, with the second surge occurring between 50–80 CC. Unlike the data from the top unit, the data recorded for the bottom unit aligned closely with design expectations and showed high stability within the 10–30 CC range.

6. Conclusion

The laboratory characterization of the babyMOSS prototype has successfully validated the functional and performance benchmarks required for the ALICE ITS3 campaigns. Through a systematic testing protocol, the sensor demonstrated reliable properties based on threshold, noise, and fake-hit rate across different operating parameters. Fundamental verification through power, register, and DAC scans confirmed that the control circuitry and communication protocols of the sensor are fully operational. Despite the damage to one of the four regions in the bottom unit, the remaining pixel

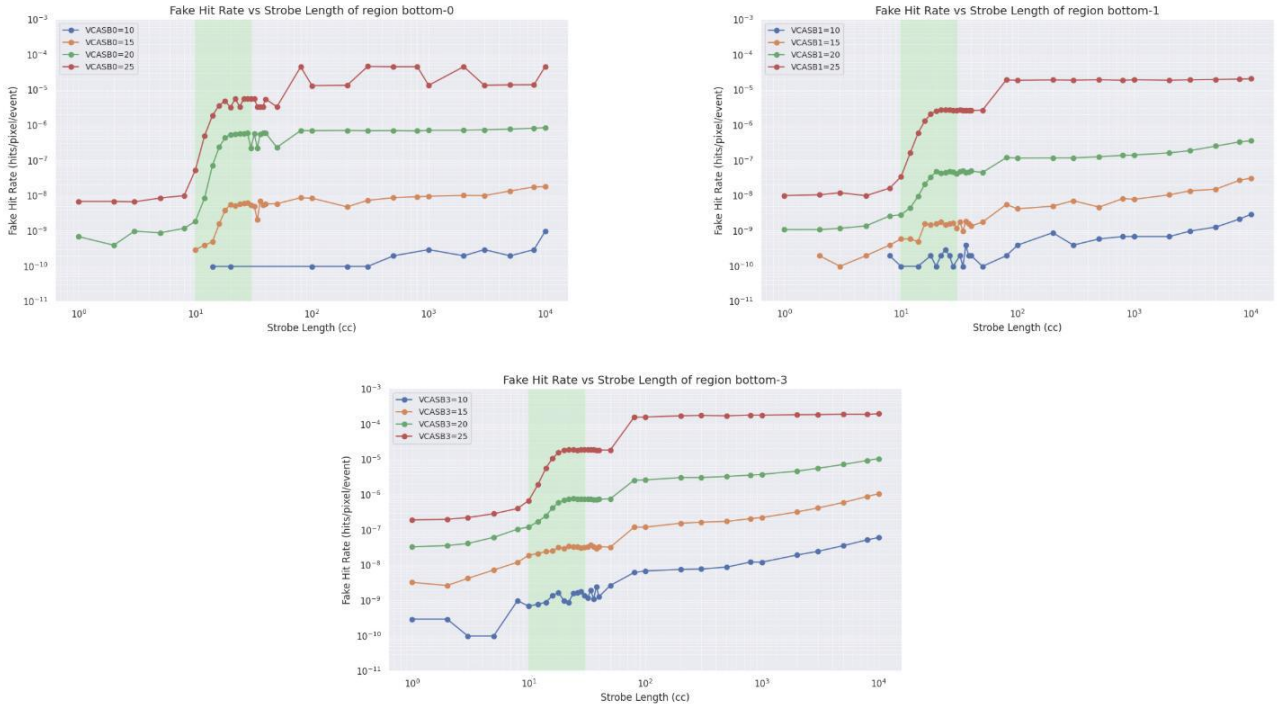

Figure 14 Relations of fake-hit rates as a function of Strobe length for different VCASB values of the bottom regions.

matrices exhibited high uniformity. Excluding the damaged region, the extracted average threshold, noise, and fake-hit rate were found to be within the desired specification range for high-precision tracking. The process to validate sensor performance is reliable and used in sensor qualification, providing a successful yield of up to 98%, excluding failures due to other sensor functions [6]. Moreover, the study of internal parameters—specifically IRESET, VCASB, IDB, and Strobe length—confirmed that the response of the sensor to biasing adjustments is consistent with the chip design expectations and performance benchmarks from other prototypes.

The results provide critical information for the MOSS/babyMOSS sensor prototypes, and the methodologies developed for this sensor model can be applied to the subsequent bent sensor prototypes of the ITS3 upgrade and the ALICE3 detectors, which are crucial for future high-energy physics studies.

7. Beneficiaries

The results detailed in this report provide significant value to several groups, as follows:

- **Pixel Sensor Researchers in Thailand:** The primary beneficiaries are scientists, researchers, and engineers focusing on the development of next-generation Monolithic Active Pixel

Sensors (MAPS) for particle detectors in high-energy physics or x-ray detectors in synchrotron light applications. The insights gained from the babyMOSS functional and parametric scans offer a critical baseline for optimizing sensor performance in future experiments.

- **The ALICE Collaboration:** This work directly supports the research and development of sensors for particle detectors under the ALICE collaboration. The results of the 65 nm CMOS stitching process validation can assist in refining and determining the final design specifications of the upcoming sensor prototype.
- **Electronic Chip Designers:** The feedback regarding the consistency of testing results with design expectations provides crucial information for the chip architects, confirming the reliability of the underlying circuitry and the manufacturing process.

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[8] babyMOSS with Raiser board: https://gitlab.cern.ch/groups/alice-its3-wp3/baby-moss/-/wikis/home

Appendix

A.1 Installation of firmware [7]

- Requirement: Python3.10 or later
- Upgrade pip and install the required packages:
  - python3 -m pip install --upgrade pip
  - python3 -m pip install -r requirements.txt
- Install package
  - make install
- Programming FPGA boards for DAQ-Raiser setup
  - Download latest tagged FPGA Firmware image from [https://gitlab.cern.ch/alice-its3-wp3/baby-moss/babymoss-daq-fpga-firmware/-/releases]
  - Download the FX3 Firmware image from [https://gitlab.cern.ch/groups/alice-its3-wp3/baby-moss/-/wikis/DAQ-Firmware-images]
- On shared machines, save .bit and .img files to /home/palpidefs/fw/
- Add udev rules from ./etc/fx3.rules to /etc/udev/rules.d.
- Trigger new udev rules
  - sudo udevadm control --reload-rules && sudo udevadm trigger
- Once firmware and software are installed, available DAQ boards can be checked by
  - raiser-daq-program --list
- Upload FX3 and FPGA firmware to the DAQ board. FX3 and FPGA firmware need to be uploaded after power cycle
  - raiser-daq-program --fx3 /path/to/img/directory/fx3.img --fpga /path/to/img/directory/raiser-daq-fpga-firmware.bit
- After the firmware upload is complete, the current read on the power supply should be about 300 mA and 350-400 mA when operating the babyMOSS chip

A.2 Command to perform functional and parametric scan [8]

- Each scan can be initiated with the following command,
    - mode_of_scan -c /path/to/your/scan_config.json5
- mode_of_scan are power_on_scan, dac_scan, register_scan, shreg_scan, analogue_scan, digital_scan, fhr_scan, and thr_scan
- option -c for scan configuration in json file
- scan_config.json5 contains scan configuration such as pixel/region/unit masking, parameter setting, bandgap trimming value, and test setup configuration (ts_config_raiser.json)

A.3 Perform bandgap trimming

- using command:
    - moss_tb moss_if *xx* trim_all_bandgaps
- *xx* is either tb for the top unit or bb for the bottom unit.
- To log bandgap, use the following command:
    - moss_tb moss_if *xx* log_dac_trimming_all_regions
- Recorded value [a,b,c,d] is a hexadecimal number.
- Trim bandgap values in the scan configuration file are in decimal units.